WHAT IS CLAIMED IS:

1. A method for generating a carry of a sum of a first and second numbers, the method comprising:

generating generate terms and propagate terms from the first and second numbers;

generating combined terms; and

generating the carry from the generate terms, the propagate terms, and the combined terms.

2. The method of claim 1, wherein

the step of generating combined terms comprises generating combined generate terms from the generate terms, and

the step of generating the carry comprises generating the carry from the generate terms, the propagate terms, and the combined generate terms.

3. The method of claim 2, wherein the step of generating combined generate terms from the generate terms comprises:

combining two of the generate terms to generate each of the combined generate terms.

4. The method of claim 3, wherein the step of combining two of the generate terms to generate each of the combined generate terms comprises:

ORing the two generate terms to generate each of the combined generate terms.

5. The method of claim 1, wherein:

the step of generating combined terms comprises generating combined generate terms and combined propagate terms from the generate terms and propagate terms, respectively; and

the step of generating the carry comprises generating the carry from the generate terms, the propagate terms, the combined generate terms, and the combined propagate terms.

6. The method of claim 5 wherein the step of generating combined propagate terms from the propagate terms comprises:

combining two of the propagate terms to generate each of the combined propagate terms.

7. The method of claim 6 wherein the step of combining two of the propagate terms to generate each of the combined propagate terms comprises:

ANDing the two propagate terms to generate each of the combined propagate terms.

8. A carry generation circuit for generating a carry of a sum of a first and second numbers, the carry generation circuit comprising:

a plurality of inputs configured to receive the first and second numbers; and

a generate and propagate term generation circuit coupled to the inputs and configured to (a) generate propagate terms, generate terms, combined generate terms, and combined propagate terms from the first and second numbers, and (b) generate the carry from the propagate terms, the generate terms, the combined generate terms, and the combined propagate terms.

9. The carry generation circuit of claim 8 wherein the generate and propagate term generation circuit comprises:

a plurality of first gates each of which configured to combine two of the generate terms to generate one of the combined generate terms.

10. The carry generation circuit of claim 8 wherein the generate and propagate term generation circuit comprises:

a plurality of second gates each of which configured to combine two of the propagate terms to generate one of the combined propagate terms.

11. A method for generating a first propagate term from a first and second operand bits, the method comprising:

providing at least a first and second gates having a dotted output; and

passing the first and second operand bits through the first and second gates, respectively, to the dotted output so as to generate the first propagate term at the dotted output.

12. The method of claim 11 further comprising:

if the first and second gates are AND gates, inverting with an inverter a signal held at the dotted output so as to generate the first propagate term.

13. The method of claim 11 wherein the step of passing the first and second operand bits through the first and second gates, respectively, to the dotted output comprises:

providing a first and second control bits to the first and second gates, respectively; and

setting the first and second control bits so as to pass the first and second operand bits through the first and second gates, respectively.

14. The method of claim 11 further comprising:

combining, with a third gate, the first propagate term and a second propagate term to generate a combined generate term.

15. A propagate term generation circuit for generating a first propagate term from a first and second operand bits, the propagate term generation circuit comprising:

at least a first and second gates having a dotted output wherein the first and second gates are configured to receive the first and second operand bits, respectively, and generate the first propagate term at the dotted output.

16. The propagate term generation circuit of claim 15 further comprising:

an inverter coupled to the dotted output and configured to invert a signal at the dotted output to generate the first propagate term, wherein the first and second gates are AND gates.

17. The propagate term generation circuit of claim 15 further comprising:

a third gate coupled to the dotted output and configured to receive the first propagate term and a second propagate term and generate a combined propagate term.

18. A method for generating a first generate term from a first bit and a second bit of a plurality of N bits, the method comprising:

providing N-1 combining gates having a dotted output;

applying the first bit to all the N-1 combining gates and applying the remaining N-1 bits including the second bit to the N-1 combining gates one-for-one; and

passing the first bit and the second bit through a first combining gate of the N-1 combining gates to the dotted output so as to generate the first generate term at the dotted output.

19. The method of claim 18 wherein the step of applying the first bit to all the N-1 combining gates comprises:

applying the first bit to all the N-1 combining gates via N-1 control gates one-for-one; and

passing the first bit through only one control gate to the first combining gate.

20. The method of claim 18 wherein the N-1 combining gates are AND gates.

21. The method of claim 18 further comprising:

combining the first generate term with a second generate term to generate a combined generate term.

22. A generate term generation circuit for generating a first generate term from a first bit and a second bit of a plurality of N bits, the generate term generation circuit comprising:

N-1 combining gates having a dotted output, the N-1 combining gates being configured to receive the first bit as their first inputs, and receive one-for-one the remaining N-1 bits including the second bit as their second inputs; wherein a first combining gate of the N-1 combining gates combines the first and second bits to generate the first generate term.

23. The generate term generation circuit of claim 22 further comprising:

N-1 control gates coupled to the N-1 combining gates one-for-one, the N-1 control gates being configured to receive the first bit and pass the first bit to only the first combining gate.

24. The generate term generation circuit of claim 22 wherein the N-1 combining gates are AND gates.

25. The generate term generation circuit of claim 22 further comprising a gate configured to combine the first generate term and a second generate term to generate a combined generate term.

26. A method for generating a carry of a sum of a first and second N-bit numbers, the method comprising:

adding, with an adder, M most significant bits of the first and second numbers to generate the carry, M being at least one but less than N.

27. The method of claim 26 wherein the step of adding comprises:

generating generate terms and propagate terms from the M most significant bits of the first and second numbers;

generating combined generate terms and combined propagate terms from the generate terms and the propagate terms, respectively; and

generating the carry from the generate terms, the propagate terms, the combined generate terms, and the combined propagate terms.

28. The method of claim 27 wherein the step of generating the propagate terms comprises:

providing at least a first and second gates having a first dotted output; and

passing a first and second bits of the first and second numbers through the first and second gates, respectively, to the first dotted output so as to generate each of the propagate terms at the first dotted output.

29. The method of claim 28 wherein the step of generating the generate terms comprises:

providing M-1 combining gates having a second dotted output;

applying a third bit of the M most significant bits of the first number to all the M-1 combining gates and applying the remaining M-1 bits including a fourth bit to the M-1 combining gates one-for-one; and

passing the third bit and the fourth bit through a first combining gate of the M-1 combining gates to the second dotted output so as to generate each of the generate terms at the second dotted output.

30. A carry generation circuit for generating a carry of a sum of a first and second N-bit numbers, the carry generation circuit comprising:

an addition circuit configured to receive M most significant bits of the first and second numbers and add the M most significant bits of the first and second numbers to generate the carry, M being at least one but less than N.

31. The carry generation circuit of claim 30 wherein the addition circuit is configured to:

generate terms and propagate terms from the M most significant bits of the first and second numbers;

generate combined generate terms and combined propagate terms from the generate terms and the propagate terms, respectively; and

generate the carry from the generate terms, the propagate terms, the combined generate terms, and the combined propagate terms.

32. The carry generation circuit of claim 31 wherein the addition circuit comprises a propagate term generation circuit including at least a first and second gates having a first dotted output, the propagate term generation circuit being configured to pass a first and second bits of the first and second numbers through the first and second gates, respectively, to the first dotted output so as to generate each of the propagate terms at the first dotted output.

33. The carry generation circuit of claim 32 wherein the addition circuit further comprises a generate term generation circuit including M-1 combining gates having a second dotted output, the generate term generation circuit being configured to:

apply a third bit of the M most significant bits of the first number to all the M-1 combining gates and applying the remaining M-1 bits including a fourth bit to the M-1 combining gates one-for-one; and

pass the third bit and the fourth bit through a first combining gate of the M-1 combining gates to the second dotted output so as to generate each of the generate terms at the second dotted output.